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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,405	12/05/2003	Esin Terzioglu	13248US02	9606

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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H1A

Office Action Summary	Application No.	Applicant(s)	
	10/729,405	TERZIOGLU ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment file don 3/4/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-73* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-47,49-52,54-61,63-69 and 71-73* is/are rejected.

7)☒ Claim(s) *48,53,62 and 70* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **44-73** are present for examination.

The last office action has been withdrawn in view of the teachings from these newly discovered arts as discussed below:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **44-47, 49-52, 54-61, 63-69, & 71-73** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Furuyama et al (5,787,046).**

Regarding claims 44, 57, 58 & 66, **Furuyama et al (see Fig. 8)** shows an addressing means for providing redundancy decoding that includes a plurality of predecoder (50, 51, 52) based on the coupled address bits (A0-A2, A3-A4, A5-A7, respectively). Thus, based on the supplied addresses bits, each corresponding predecoder is activated or selected and their outputs is coupled to the main decoder (53), and thus it would have been obvious to one skilled in this art that when/if one decoder is selected, it's predecoded address input lines are also shifted into work, and the other two decoders are shifted out as inactive or idles state. For example, Fig. 12 shows in detail the structure of a predecoder

(50), see also cols. 8-9, wherein the redundant selector (31) is provided with 8 switching circuits (A) and redundant address comparators (36) for activating the proper predeocoder's output signals based on the supplied input address bits (A0 to A2). Thus, with regard to the "shifting" terminology" as concern, although this reference does not explicitly state that term anywhere; however, the analogous use of particular applied address bits (upper and lower 3 bits) in this reference obviously acting as 'control" bits for activating or "shifting in" only one predecoder's address lines for active use while still be able to deactivating or "shifting out" the other predecoder lines from the two non-active predecoders based on supplied address bits. Thus, one skilled in this art can obvious infer the knowledge of "shifting out" one predecoder and "shifting in" the other predecoder as a substitute or a replacement one (based on redundancy address bits) is already implied by this teaching.

Regarding claims 46, 51, 56, 65, 60, 68, and 73, Fig. 12 shows the use of redundant selector circuit (31) as means for shifting in and shifting out the right decoder at a time.

Regarding claims 47, 52, 61 & 69Fig. 8 shows at least the third predecoder has higher address predecoded lines or bits coupled to its inputs (A0 to A7);

Regarding claims 49 & 57, Fig. 12 shows the use of address comparators for identifying the use of proper predecoder to be used based on supplied address bits (A0 to A7, Fig. 8) and also the redundant addresses setting circuits (i.e., programmed fuses for defective cells., col. 8, lines 50-65);

Regarding claims 54, 55, 63, 64, 71 & 72, Fig. 12 shows the use of redundant selector and compare circuits and switching circuits adapted for firing any address mappings;

4. Claims **44-47, 49-52, 54-61, 63-69, & 71-73** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wendell et al (5,841,712).**

Regarding claims 44, 57, 58 & 66, **Wendell et al (see Fig. 4)** shows a redundant addressing means for providing redundancy address decoding that includes a plurality of predecoders (410, 411, 412) based on the coupled address bits (RA0 to RA7, respectively). Thus, based on the supplied addresses bits, each corresponding predecoder is activated or selected and their outputs is coupled to the main row decoder (201), and thus it would have been obvious to one skilled in this art that when/if one decoder is selected, it's predecoded address input lines are also shifted into work, and the other two decoders are shifted out as inactive or idles state. For example, Fig. 4 shows in detail the structure of a address shifting circuitry (using NOT comparators 402 and AND gate 405), wherein this whole circuitry is provided with output switching/predeocded lines coupled to the inputs of three predecoders (410 to 412) in order to activate or shift in a proper predecoder to be used (based on the supplied input address bits (A0 to A2)). Thus, with regard to the "shifting" terminology" as concern, although this reference does not explicitly state that term anywhere; however, the analogous use of particular applied address bits (upper and lower 3 bits) in this

reference obviously acting as 'control" bits for activating or "shifting in" only one predecoder for active use while still be able to deactivating or "shifting out" the other two non-active predecoders based on supplied address bits. Thus, one skilled in this art can obvious infer the knowledge of "shifting out" one predecoder and "shifting in" the other predecoder as a substitute or a replacement one (based on redundancy address bits) is already implied by this teaching.

Regarding claims 46, 51, 56, 65, 60, 68, and 73, Fig. 4 shows the use of comparator circuit (31) as means for shifting in and shifting out the right decoder at a time base don supplied row address identified as "failed (406, 407)".

Regarding claims 47, 52, 61 & 69, Fig. 4 shows at least one predecoder (412) has higher address predecoded lines or bits coupled to its inputs (RA4 to RA7);

Regarding claims 49 & 57, Fig. 4 shows the use of address comparators for identifying the use of proper predecoder to be used based on supplied address bits (RA0 to RA7) and also the redundant addresses setting circuits (404, 414);

Regarding claims 54, 55, 63, 64, 71 & 72, Fig. 4 shows the use of redundant selector and compare circuits and switching circuits adapted for firing any address mappings;

5. Claims **44-47, 49-52, 54-61, 63-69, & 71-73** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Saruwatari (5,243,570).**

Saruwatari (see Fig. 3) shows an addressing means for providing redundancy decoding that includes a plurality of predecoders (14a, 14b, 15b) based on the

coupled address bits (Y1 to Y4, respectively). Thus, based on the supplied addresses bits, each corresponding predecoder is activated or selected (by the shown program circuit 15a) and their respective outputs is coupled to the main decoders (RDC or DC1-32), and thus it would have been obvious to one skilled in this art that when/if one decoder is selected, it's predecoded address input lines (Y0-Y4) are also shifted into work, and the other two decoders are shifted out as inactive or idles state. For example, Fig. 4 shows in detail the structure of a predecoder (50), see also cols. 8-9, wherein the redundant selector (31) is provided with 8 switching circuits (A) and redundant address comparators (36) for activating the proper predeocoder's output signals based on the supplied input address bits (A0 to A2). Thus, with regard to the "shifting" terminology" as concern, although this reference does not explicitly state that term anywhere; however, the analogous use of particular applied address bits (upper and lower 3 bits) in this reference obviously acting as 'control" bits for activating or "shifting in" only one predecoder's address lines for active use while still be able to deactivating or "shifting out" the other predeocded lines from the two non-active predecoders based on supplied address bits. Thus, one skilled in this art can obvious infer the knowledge of "shifting out" one predecoder and "shifting in" the other predecoder as a substitute or a replacement one (based on redundancy address bits) is already implied by this teaching.

6. Other claims contain allowable subject matter over prior arts of record for the following reasons:

Claims **48, 53, 62, and 70** recites the features of "at least lower address predecoded line coupled to at least one of said at least one predecoder and said at least other predecoder and paired with said at least one higher address predecoder line" which is not fairly seen or suggested elsewhere.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827